



# 1.2 Micron CMOS Process Family

March 1997

## Features

- Double Poly/Double Metal
- 2.4  $\mu\text{m}$  Poly and Metal I Pitch
- 5.5 Volts Maximum Operating Voltage
- Twin-tub process on P-type wafers
- ProToDuction™ Option for low cost prototypes

## Description

The 1.2 $\mu\text{m}$  process provides flexibility, speed and packing density needed in mixed signal designs. The aggressive design rules on both metal layers are comparable to most 0.8 $\mu\text{m}$  processes. Also, the overall design rules are compatible with most other 1.2 $\mu\text{m}$  processes making second sourcing easy.

## Technology Outline

- Twin-tub technology
- Drain Engineered Structure to Ensure Reliability against Hot-Carrier Injection
- Planarization with non-etch-back SOG Processes
- State-of-the-art Metal technology :Ti/TiN/Al/TiN sandwich
- Plasma Silicon Nitride Passivation for Reliability against moisture
- Latchup Free Process on Non-Epi material achieved

## Process Parameters

Process Parameters	1.2 $\mu\text{m}$ 5volts	Units
Metal I pitch (width/space)	1.4/1.0	$\mu\text{m}$
Metal II pitch (width/space)	1.4/1.0	$\mu\text{m}$
Poly pitch (width/space)	1.2/1.2	$\mu\text{m}$
Contact	1.2x1.2	$\mu\text{m}$
Via	1.4x1.4	$\mu\text{m}$
Gate geometry	1.2	$\mu\text{m}$
N-well junction depth	4.0	$\mu\text{m}$
P-well junction depth	4.0	$\mu\text{m}$
N+ junction depth	0.20	$\mu\text{m}$
P+ junction depth	0.31	$\mu\text{m}$
Gate oxide thickness	225	Å
Inter poly oxide thick.	390	Å

## MOSFET Electrical Parameters

Electrical Parameters	1.2 MICRON - 5 volts						Units	Conditions
	N Channel			P Channel				
	min.	typ.	max.	min.	typ.	max.		
Vt (10x1.2 $\mu\text{m}$ )	0.55	0.70	0.85	0.55	0.70	0.85	V	saturation
I <sub>ds</sub> (10x1.2 $\mu\text{m}$ )		240			140		$\mu\text{A}/\mu\text{m}$	V <sub>ds</sub> =V <sub>gs</sub> =5v
Gain $\beta$ (10x10 $\mu\text{m}$ )		73			24		$\mu\text{A}/\text{V}^2$	
Body Factor (50x50 $\mu\text{m}$ )		0.56			0.73		$\sqrt{v}$	
Bvdss	10	15		10	12		V	I <sub>ds</sub> =20nA
Subthreshold Slope		90			90		mV/dec.	V <sub>ds</sub> =0.1v
Maximum Substrate Current (50x1.2 $\mu\text{m}$ )		0.20			.01		$\mu\text{A}/\mu\text{m}$	V <sub>ds</sub> =5.5v V <sub>gs</sub> =2.7v
Field Threshold	10	25		10	25		V	I <sub>ds</sub> = 14 $\mu\text{A}$
L Effective		1.0			0.82		$\mu\text{m}$	L drawn = 1.5 $\mu\text{m}$

# 1.2 Micron CMOS Process Family

## Capacitances (fF/ $\mu\text{m}^2$ )

	min.	typ.	max
Inter-poly	0.80	0.97	1.15
Gate oxide	1.4	1.5	1.6
N+ Junction		0.35	
P+ Junction		0.60	

## Bipolar gain<sup>1</sup>

	min.	typ.	max.
NPN vertical		80	
PNP vertical		10	

<sup>1</sup>Test condition : Vce = 5 volts

## Resistances ( $\Omega/\text{sq.}$ )

	min.	typ.	max.
Nwell		520	
Pwell		2300	
N+	35	45	55
P+	80	100	120
Poly gate	15	20	25
Poly capacitor	75	100	125
Metal I		0.038	
Metal II		0.038	

FIG 1 : I-V Characteristics for a 50x1.2 $\mu\text{m}$  N-MOSFET

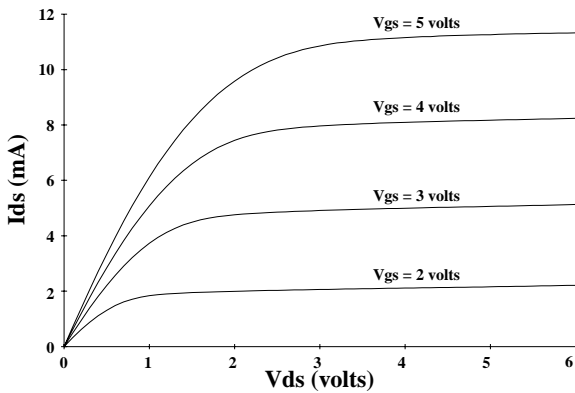


FIG 2 : I-V Characteristics for a 50x1.2 $\mu\text{m}$  P-MOSFET

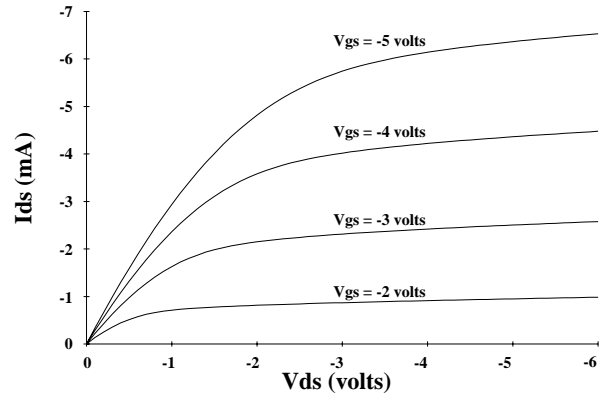


FIG 3 : Subthreshold Characteristics at Vds=0.1 volt for a 50x1.2 $\mu\text{m}$  N-MOSFET

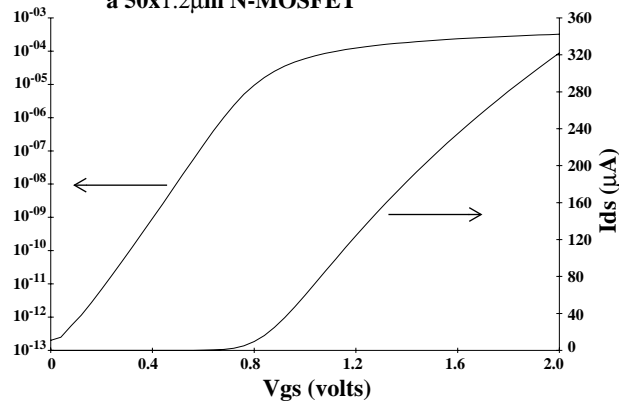
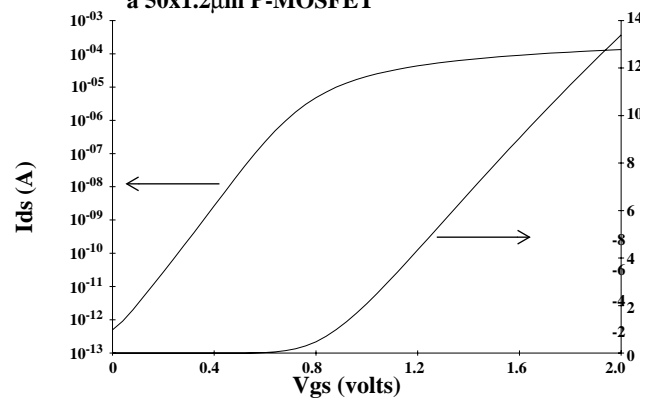


FIG 4 : Subthreshold Characteristics at Vds=-0.1 volt for a 50x1.2 $\mu\text{m}$  P-MOSFET



NOTE : These values are for guidance only. Many of them can be adjusted to suit customer requirements. For full process specifications contact a Mitel sales office or representative.